

UNITED STATES PATENT APPLICATION

SYSTEM AND METHOD FOR CHANNELIZATION RECOGNITION IN A
WIDEBAND COMMUNICATION SYSTEM

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SYSTEM AND METHOD FOR CHANNELIZATION RECOGNITION IN A WIDEBAND COMMUNICATION SYSTEM

Technical Field

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The present invention pertains to wireless communications. Some embodiments of the present invention pertain to wireless local-area networks (WLANs) and high-throughput (HT) orthogonal frequency-division multiplexed (OFDM) communications.

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Background

Orthogonal frequency-division multiplexing (OFDM) is an example of a multi-carrier transmission technique that uses symbol-modulated orthogonal subcarriers to transmit information within an available spectrum. Many modern digital communication systems, including wireless local-area networks (WLANs), are using symbol-modulated orthogonal subcarriers as a modulation scheme to help signals survive in environments having multipath reflections and/or strong interference. One problem with many conventional systems that use symbol-modulated subcarriers is that channel bandwidth is limited to the bandwidth of the individual channels. Some conventional wireless communication systems, such as WLANs that implement OFDM communications, communicate using channels that may only have about a 20 MHz bandwidth. Thus, there are general needs for systems and methods for wider bandwidth communications.

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Brief Description of the Drawings

The appended claims are directed to some of the various embodiments of the present invention. However, the detailed description presents a more complete understanding of embodiments of the present invention when considered in connection with the figures, wherein like reference numbers refer to similar items throughout the figures and:

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FIG. 1 is a block diagram of a wideband receiver system in accordance with some embodiments of the present invention;

FIG. 2 is a block diagram of a portion of short-training symbol processing circuitry in accordance with some embodiments of the present invention;

5 FIG. 3 is block diagram of portions of data-symbol processing circuitry in accordance with some embodiments of the present invention;

FIG. 4 is block diagram of portions of data-symbol processing circuitry in accordance with other embodiments of the present invention;

10 FIG. 5 is a block diagram of RF-receive circuitry in accordance with some embodiments of the present invention;

FIG. 6 illustrates matched-filter coefficient spectra in accordance with some embodiments of the present invention;

FIG. 7 illustrates filter response of matched filters in accordance with some embodiments of the present invention; and

15 FIG. 8 is a flow chart of a channelization-identification procedure in accordance with some embodiments of the present invention.

Detailed Description

20 The following description and the drawings illustrate specific embodiments of the invention sufficiently to enable those skilled in the art to practice them. Other embodiments may incorporate structural, logical, electrical, process, and other changes. Examples merely typify possible variations. Individual components and functions are optional unless explicitly required, and
25 the sequence of operations may vary. Portions and features of some embodiments may be included in or substituted for those of others. The scope of embodiments of the invention encompasses the full ambit of the claims and all available equivalents of those claims.

30 FIG. 1 is a block diagram of a wideband receiver system in accordance with some embodiments of the present invention. Receiver system 100 may comprise radio frequency (RF) receiver circuitry 102 to receive symbol-modulated subcarriers through antenna 114 and to generate serial symbol stream 104. Receiver system 100 may also comprise data-symbol processing circuitry

110 to process serial symbol stream 104 and generate decoded bit stream 112.

Receiver system 100 may also comprise short-training symbol processing circuitry 106 which may receive serial symbol stream 104 and may generate channelization vector 108 for use by data-symbol processing circuitry 110.

5 In accordance with some embodiments, short-training symbol processing circuitry 106 may determine the channelization of a wideband channel by detecting a plurality of subchannels and may generate channelization vector 108 indicating which of the subchannels are active and which of the subchannels are inactive. In response to the channelization vector, data-symbol processing
10 circuitry 110 may process symbols from the active subchannels and may refrain from processing the inactive subchannels. Attempting to receive on an inactive channel may result in loss of the entire packet, especially when the inactive channel contains noise and/or interference. In some embodiments, data-symbol processing circuitry 110 may refrain from processing the inactive subchannels by
15 switching-off or turning-off processing for the inactive subchannels.

 In some embodiments, decoded bit stream 112 may be generated from the combined contributions of the active channels. In some embodiments, the subchannels may be detected with a parallel set of matched filters. The matched filters may have coefficient spectra matched to corresponding ones of the
20 subchannels. Some of these embodiments are described in more detail below.

 In some embodiments, short-training symbol processing circuitry 106 may perform functions such as packet detection and synchronization with symbol boundaries. In some embodiments, short-training symbol processing circuitry 106 may initiate data processing by data-symbol processing circuitry
25 110, although the scope of the invention is not limited in these respects.

 In some embodiments, receiver system 100 may be part of a wireless communication device which receives and/or transmits RF communications with antenna 114. Examples of a wireless communication device may include a personal digital assistant (PDA), a laptop or portable computer with wireless
30 communication capability, a web tablet, a wireless telephone, a wireless headset, a pager, an instant messaging device, an MP3 player, a digital camera, an access point or other device that may receive and/or transmit information wirelessly. In some embodiments, receiver system 100 may receive RF communications in

accordance with specific communication standards, such as the IEEE 802.11(a), 802.11(b), 802.11(g) and/or 802.16 standards for wireless local-area network communications, including high-throughput (HT) and wideband (WB) standards.

In some embodiments, antenna 114 may comprise a directional or
5 omnidirectional antenna, including, for example, a dipole antenna, a monopole antenna, a loop antenna, a microstrip antenna or other type of antenna suitable for reception and/or transmission of RF signals.

Accordingly, receiver system 100 may operate as part of a WB or HT OFDM communication system. In some embodiments, receiver system 100 may
10 provide for recognition of a channelization configuration in WB or HT OFDM systems, including systems with an adaptively-changing frequency bandwidth. In these embodiments, the bandwidth of a communication channel may be increased by combining up to four or more narrowband channels (e.g., subchannels) to form a wideband channel. In some embodiments, the
15 subchannels may have bandwidths of approximately 20 MHz, and the wideband channel may have a bandwidth of up to 80 MHz and greater depending on the number of subchannels utilized.

In some embodiments, a transmitting communication station, (e.g., an HT access point) may dynamically select the wideband channel bandwidth and may
20 avoid subchannels with poor quality or other problems. In these embodiments, a transmitting communication station may employ a parallel multichannel data transmission technique which uses one or more subchannels with synchronized data streams. In these embodiments, each data stream may be preceded by a standard preamble, such as an 802.11a preamble, although the scope of the
25 invention is not limited in this respect. Receiver system 100 may not know in advance which particular subchannels the transmitting station is utilizing for transmitting a wideband packet. Therefore, receiver system 100 may sample the subchannels to generate channelization vector 108 to identify which subchannels are active and which subchannels are inactive.

30 Although receiver system 100 is illustrated as having several separate functional elements, one or more of the functional elements may be combined and may be implemented by combinations of software-configured elements, such as processing elements including digital signal processors (DSPs), and/or other

hardware elements. For example, some of the illustrated elements may comprise one or more microprocessors, DSPs, application specific integrated circuits (ASICs), and combinations of various hardware and logic circuitry for performing at least the functions described herein.

5 FIG. 2 is a block diagram of a portion of short-training symbol processing circuitry in accordance with some embodiments of the present invention. Short-training symbol processing circuitry 200 may be suitable for use as short-training symbol processing circuitry 106 (FIG. 1), although other circuitry may also be suitable. Short-training symbol processing circuitry 200 may detect a training
10 sequence (e.g., serial symbol stream 104 (FIG. 1) comprising a sampled short-training sequence) modulated on one or more subchannels and may generate channelization vector 208 indicating which of the subchannels are active and which of the subchannels are inactive. In some embodiments, short-training symbol processing circuitry 200 may comprise filter bank 202 having a plurality
15 of matched filters 206. Each matched filter 206 may have a coefficient spectrum matched to a corresponding one of the subchannels.

 In some embodiments, short-training symbol processing circuitry 200 may further comprise non-coherent summaters 210 to sum output from a corresponding one of matched filters 206, and threshold detectors 212 to
20 determine when the summed output from a corresponding one of summaters 210 exceeds a predetermined threshold. Non-coherent summaters 210 do not preserve the magnitude and phase of the signals in summation. Short-training symbol processing circuitry 200 may further comprise multiplexer 214 to combine outputs from threshold detectors 212 to assemble channelization vector
25 208. In some embodiments that utilize four subchannels comprising a wideband channel, multiplexer, for example, may assemble a channelization vector, such as "1011", that may indicate that the first, third and fourth subchannels are active and that the second subchannel is inactive.

 In some embodiments, the number of matched filters 206, summaters 210
30 and threshold detectors 212 may depend on the number of subchannels that comprise a wideband channel. Although short-training symbol processing circuitry 200 is illustrated with four matched filters 206, four summaters 210 and four threshold detectors 212, the scope of the invention is not limited in this

respect. In some embodiments, channelization vector 208 may include a “one” or a “zero” for each subchannel of a wideband channel.

In some embodiments, filters 206 may be matched to a short training OFDM symbol, such as the short-training symbols of the 802.11a standard. In
5 these embodiments, each filter 206 may have substantially the same filter coefficients, but their center frequencies may be shifted by the frequency offset between the channels, such as about approximately 20 MHz. Examples of this are further described below.

In some embodiments, non-coherent summators 210 may perform an
10 averaging of the matched-filter response over several of the short-training symbols. This may reduce noise and accumulate energy from subsequent short-training symbols. In some embodiments, threshold detectors 212 may be threshold devices that search for a threshold exceeding a predetermined amount within a predetermined symbol interval. In some embodiments, the beginning of
15 the symbol interval may be determined at a wideband energy-detection instant (e.g., when a wideband packet is initially detected). In some embodiments, detection, automatic gain control (AGC), and coarse frequency estimation may be performed over all available subchannels. The signals from different subchannels may be combined (e.g., optimally weighted) to obtain a single AGC
20 value and a single frequency estimate offset for processing the packet.

In some embodiments, sampled short-training sequence 204 is provided to matched filters 206 after receiver system 100 (FIG. 1) detects a wideband packet and performs a coarse frequency offset correction using the first several of the short-training symbols. In some embodiments, the thresholds for threshold
25 detectors 212 may be calculated from a Neyman-Pearson criterion for a predetermined false-alarm probability, although the scope of the invention is not limited in this respect.

In some embodiments, the generation of channelization vector 208 may also be used for coarse symbol-timing synchronization. In these embodiments,
30 coarse timing synchronization may be performed by matched filtering the last short symbols of the short-training sequence so that the moment threshold devices 212 detect a threshold exceeding a predetermined threshold, the boundary of the training symbols may be determined.

The independent detection of subchannels with non-coherent summators 210 may provide a greater stability to multi-path distortion, especially in a frequency-selective channel. The use of a parallel set of identical or substantially identical matched filters 206 may reduce filter length and reduce complexity
5 compared with conventional maximum-likelihood channel-recognition schemes. Although in some embodiments, matched filters 206 are described as being matched to a sequence of short-training symbols of known values, this is not a requirement. Matched filters 206 may be matched to any predetermined sequence.

10 FIG. 3 is a block diagram of a portion of data-symbol processing circuitry in accordance with some embodiments of the present invention. Data-symbol processing circuitry 300 may be suitable for use as data-symbol processing circuitry 110 (FIG. 1), although other circuitry may also be suitable. Data-symbol processing circuitry 300 processes serial symbol stream 304 of OFDM symbols
15 to generate a decoded bit stream 312. In accordance with some embodiments, data-symbol processing circuitry 300 may be responsive to channelization vector 308 and may process data symbols on subchannels identified as active subchannels. Accordingly, decoded bit stream 312 may represent data from one or more active subchannels. In some embodiments, data-symbol processing
20 circuitry 300 may actively refrain from processing on subchannels identified as inactive subchannels.

Data-symbol processing circuitry 300 may include serial-to-parallel converter 302 to convert a symbol of serial symbol stream 304 into parallel groups of time-domain samples 306 for fast-Fourier transform (FFT) circuitry
25 309. FFT circuitry 309 may perform a FFT on the parallel groups of time-domain samples 306 to generate frequency-domain symbol-modulated subcarriers 310. In some embodiments, FFT circuitry 309 may perform an FFT on known training symbols (e.g., long-training symbols) so that a channel estimate may be generated for the subchannel. Channel equalizer 314 may perform channel
30 equalization on frequency-domain symbol-modulated subcarriers 310 and may generate channel-equalized frequency-domain symbol-modulated subcarriers 316. Channel equalizer 314 and may use the channel estimation provided by a channel estimator (not illustrated). In some embodiments, channel equalizer 314

may perform channel equalization in the frequency domain by division of the frequency domain subcarriers 310 with complex values that represent the channel estimation provided by a channel estimator. Accordingly, the magnitudes of equalized frequency-domain symbol-modulated subcarriers 316
5 may be normalized and the phases of equalized frequency-domain symbol-modulated subcarriers 316 may be aligned to a zero origin to allow for further processing by demapper and deinterleaver circuitry 318.

In some embodiments, equalized frequency-domain symbol-modulated subcarriers 316 may be demodulated by a demodulator (not separately
10 illustrated) to produce a plurality of demodulated parallel symbols. In some embodiments, the demodulator may individually demodulate the individual subcarriers in accordance with a particular modulation order in which the transmitter individually modulated the subcarriers. Modulation orders, for example, may include binary phase shift keying (BPSK), which communicates
15 one bit per symbol, quadrature phase shift keying (QPSK), which communicates two bits per symbol, 8PSK, which communicates three bits per symbol, 16-quadrature amplitude modulation (16-QAM), which communicates four bits per symbol, 32-QAM, which communicates five bits per symbol, and 64-QAM, which communicates six bits per symbol. Modulation orders may also include
20 differentially-coded star QAM (DSQAM). Modulation orders with lower and even higher communication rates may also be used by the transmitting station. The parallel symbols from the demodulator may be converted from a parallel form to a serial stream and provided to demapper and deinterleaver circuitry 318.

Demapper and deinterleaver circuitry 318 may demap and deinterleave
25 the demodulated frequency-domain symbol-modulated subcarriers 316 to generate bit stream 320 which may be decoded by decoder 326. Decoder 326 may be a Viterbi decoder, although the scope of the invention is not limited in this respect.

In accordance with some embodiments of the present invention, data-
30 symbol processing circuitry 300 may also include circuitry for processing a predetermined number of subchannels in parallel. Although FIG. 3 illustrates data-symbol processing circuitry 300 with elements for processing four subchannels in parallel, this is not a requirement, and in some embodiments,

data-symbol processing circuitry 300 may include elements for processing an even greater number of subchannels. In these embodiments, combiner 322 may combine the bit streams generated from each subchannel and provide combined bit stream 324 to decoder 326.

5 In some embodiments, when RF-receive circuitry 102 provides separate serial symbol streams 304 for more than one subchannel, data-symbol processing circuitry 300 may include more than one serial-to-parallel converter 302. In accordance with some embodiments, data-symbol processing circuitry 300 may comprise four 64 bit FFT circuits arranged in parallel corresponding to FFT
10 circuitry 309 for processing each of a predetermined number of subchannels substantially in parallel, although the scope of the invention is not limited in this respect.

FIG. 4 is a block diagram of a portion of data-symbol processing circuitry in accordance with other embodiments of the present invention. Data-symbol
15 processing circuitry 400 may be suitable for use as data-symbol processing circuitry 110 (FIG. 1), although other circuitry may also be suitable. Data-symbol processing circuitry 400 processes serial symbol stream 404 of OFDM symbols to generate decoded bit stream 412. In accordance with some embodiments, data-symbol processing circuitry 400 may be responsive to channelization vector 408
20 and may process data symbols on subchannels identified as active subchannels. Accordingly, decoded bit stream 412 may represent data from one or more active subchannels. In some embodiments, data-symbol processing circuitry 400 may actively refrain from processing on subchannels identified as inactive subchannels.

25 Data-symbol processing circuitry 400 may include serial-to-parallel converter 402 to convert a symbol of serial symbol stream 404 into parallel groups of time-domain samples 406 for wideband fast-Fourier transform (FFT) circuitry 409. Time-domain samples 406 may comprise time-domain samples from a wideband channel. Wideband FFT circuitry 409 may perform a FFT on
30 the parallel groups of time-domain samples 406 to generate frequency-domain symbol-modulated subcarriers 410. Wideband channel equalizer 414 may perform channel equalization on frequency-domain symbol-modulated

subcarriers 410 for each of the subchannels and may generate channel-equalized frequency-domain symbol-modulated subcarriers 416.

After demodulation, wideband demapper and deinterleaver circuitry 418 may demap and/or deinterleave the demodulated frequency-domain symbol-modulated subcarriers to generate bit stream 420 which may be decoded by
5 wideband decoder 426. Bit stream 420 may be comprised of bit-stream contributions from the active subchannels that may comprise a packet, such as an OFDM packet. Decoder 426 may be Viterbi decoder, although the scope of the invention is not limited in this respect.

10 In some embodiments, wideband FFT circuitry 409 may be a 256-bit FFT circuit configured to perform an FFT on parallel groups of time-domain samples from four subchannels, although the scope of the invention is not limited in this respect. In these embodiments, wideband FFT circuitry 409 may be responsive to channelization vector 408 to perform an FFT on the parallel groups of time-
15 domain samples from the active subchannels, and refrain from performing an FFT on the inactive channels. Although wideband FFT circuitry 409 is illustrated as being responsive to channelization vector 408, other elements of data-symbol processing circuitry 400 may also be responsive to channelization vector 408.

FIG. 5 is a block diagram of RF-receive circuitry in accordance with
20 some embodiments of the present invention. RF-receive circuitry 500 may be suitable for use as RF-receive circuitry 102 (FIG. 1) although other circuitry may also be suitable. RF-receive circuitry 500 may perform a two-stage downconversion, although this is not a requirement. RF-receive circuitry 500 may include low-noise amplifier (LNA) 512 and RF downconverter 514. RF
25 downconverter 514 may generate an intermediate frequency (IF) signal using signals from oscillator 516. Oscillator 516 may be a fixed-frequency heterodyne oscillator. Automatic gain control (AGC) element 518 may adjust a power level for IF down converter 520. IF down converter 520 may generate baseband signals, and in some embodiments, may function as a detector to generate in-
30 phase (I) signals and quadrature phase (Q) signals at substantially zero frequency using a frequency controllable device such as voltage-controlled oscillator (VCO) 522. In one embodiment, VCO 522 may be set upon detection of a wideband OFDM packet and may remain constant for the duration of the

wideband OFDM packet. The in-phase (I) signals and quadrature phase (Q) signals, provided by IF down converter 520, may be sampled and converted to a digital bit stream by analog to digital converter (ADC) 526 to provide serial symbol stream 504.

5 In accordance with some embodiments of the present invention, RF-receive circuitry 500 may generate serial symbol stream 504 from one or more received subchannels that comprise a wideband channel. In these embodiments, RF-receive circuitry 500 may generate a single time-division multiplexed serial symbol stream (i.e., serial symbol stream 504) which may be provided to
10 matched filters 206 (FIG. 2). This single time-division multiplexed serial symbol stream may include a serial symbol stream from more than one of the subchannels. In these embodiments LNA 512 and RF downconverter 514 may operate over up to four of more of the subchannels.

 In accordance with other embodiments of the present invention, RF-
15 receive circuitry 500 may comprise separate elements for each of the subchannels to generate parallel sets of serial symbol streams (e.g., one for each received subchannel). For example, more than one ADC 526, among other things, may be included as part of circuitry 500. In these embodiments, the individual serial symbol streams may be provided separately to each of matched
20 filters 206 (FIG. 2).

 FIG. 6 illustrates matched-filter coefficient spectra in accordance with some embodiments of the present invention. Coefficient spectra 600 illustrate coefficient spectra of four matched filters which may be suitable in some embodiments which detect up to four subchannels in parallel. Embodiments of
25 the present invention are equally suitable with the use of less than four or more than four matched filters. Furthermore, coefficient spectra 600 are illustrated for subchannels having a 20 MHz bandwidth, although the scope of the invention is not limited in this respect. In some embodiments, the matched filters may have identical or substantially identical coefficients, but may have their center
30 frequencies shifted depending on the location of the subchannels.

 Coefficient spectrum 602 illustrates a coefficient spectrum for a matched filter having its center frequency offset by negative 30 MHz from wideband-channel center frequency 610. Coefficient spectrum 602 may represent a

coefficient spectrum of a first of a plurality of matched filters, such as a first one of matched filters 206 (FIG. 2). Coefficient spectrum 604 illustrates a coefficient spectrum for a matched filter having its center frequency offset by negative 10 MHz from wideband-channel center frequency 610. Coefficient spectrum 604
5 may represent a coefficient spectrum of a second of a plurality of matched filters, such as a second one of matched filters 206 (FIG. 2). Coefficient spectrum 606 illustrates a coefficient spectrum for a matched filter having its center frequency offset by positive 10 MHz from wideband-channel center frequency 610. Coefficient spectrum 606 may represent a coefficient spectrum of a third of a
10 plurality of matched filters, such as a third one of matched filters 206 (FIG. 2). Coefficient spectrum 610 illustrates a coefficient spectrum for a matched filter having its center frequency offset by positive 30 MHz from wideband-channel center frequency 610. Coefficient spectrum 610 may represent a coefficient spectrum of a fourth of a plurality of matched filters, such as a fourth one of
15 matched filters 206 (FIG. 2).

FIG. 7 illustrates filter responses of matched filters in accordance with some embodiments of the present invention. Filter responses 702 through 708 may illustrate the filter responses over time for four matched filters, such as filters 206 (FIG. 2), when used as part of circuitry 200 (FIG. 2) for generating a
20 channelization vector, such as channelization vector 208 (FIG. 2). FIG. 7 illustrates the generation of channelization vector "1001". Filter response 702 of a first matched filter is illustrated as exceeding threshold 712 which may provide a "1" in the first position of the channelization vector. Filter response 704 is illustrated as not exceeding threshold 712 which may provide a "0" in the second
25 position of the channelization vector. Filter response 706 is illustrated as not exceeding threshold 712 which may provide a "0" in the third position of the channelization vector. Filter response 708 is illustrated as exceeding threshold 712 which may provide a "1" in the fourth position of the channelization vector. The generation of channelization vector "1001" may indicate that the first and
30 fourth subchannels are active and that the second and third subchannels are inactive.

FIG. 8 is a flow chart of a channelization-identification procedure in accordance with embodiments of the present invention. Procedure 800 may be

used as part of wideband receiver which receives symbol-modulated communications over a wideband channel that may be adaptively changed by a transmitting station. In some embodiments, procedure 800 may be performed by a wideband receiver system, such as receiver system 100 (FIG. 1), although other
5 receivers may also be suitable for performing procedure 800. Although the individual operations of procedure 800 are illustrated and described as separate operations, one or more of the individual operations may be performed concurrently and nothing requires that the operations be performed in the order illustrated.

10 Operation 802 receives subchannels of a plurality of subchannels that may comprise a wideband channel. Operation 802 may include receiving synchronized sequences of training symbols (such as short-OFDM training symbols) over more than one subchannel, although the scope of the invention is not limited in this respect. Operation 802 may generate a serial symbol stream,
15 such as serial symbol stream 104 (FIG. 1), and, in some embodiments, operation 802 may generate a sampled short-training sequence such as sampled short-training sequence 204 (FIG. 2). In some embodiments, operation 802 may be performed by RF-receive circuitry 102 (FIG. 1), although the scope of the invention is not limited in this respect.

20 Operation 804 generates a channelization vector from the serial symbol stream. The channelization vector may indicate which of the subchannels are active and which are inactive. Operation 804 may generate the channelization vector using a matched coefficient spectrum for the subchannels. In some embodiments, operation 804 may be performed by short-training symbol
25 processing circuitry 106 (FIG. 1), although the scope of the invention is not limited in this respect.

 Operation 806 may perform data-symbol processing on the active subchannels. In some embodiments, operation 806 may actively refrain from performing data-symbol processing on the inactive subchannels by switching-off
30 the processing circuitry, such as FFT circuitry, for the inactive channels. In some embodiments, operation 806 may be performed by data-symbol processing circuitry 110 (FIG. 1) in response to the channelization vector, although the scope of the invention is not limited in this respect.

Operation 808 generates a combined bit stream representing contributions from the active subchannels, and operation 810 decodes the combined bit stream to generate a decoded bit stream, such as decoded bit stream 112 (FIG. 1). In some embodiments, operations 808 and 810 may be performed
5 by data-symbol processing circuitry 110 (FIG. 1), although the scope of the invention is not limited in this respect.

In some embodiments, operations 802 through 804 may be performed using the sequence of short-training symbols of the preamble of an OFDM packet, and operation 806 through 810 may be performed using the long-training
10 symbols and data symbols of the OFDM packet. In some embodiments, operations 802 through 810 may be repeated for each subsequently received packet.

Unless specifically stated otherwise, terms such as processing, computing, calculating, determining, displaying, or the like, may refer to an
15 action and/or process of one or more processing or computing systems or similar devices that may manipulate and transform data represented as physical (e.g., electronic) quantities within a processing system's registers and memory into other data similarly represented as physical quantities within the processing system's registers or memories, or other such information storage, transmission
20 or display devices. Furthermore, as used herein, computing device includes one or more processing elements coupled with computer readable memory that may be volatile or non-volatile memory or a combination thereof.

Embodiments of the invention may be implemented in one or a combination of hardware, firmware and software. Embodiments of the invention
25 may also be implemented as instructions stored on a machine-readable medium, which may be read and executed by at least one processor to perform the operations described herein. A machine-readable medium may include any mechanism for storing or transmitting information in a form readable by a machine (e.g., a computer). For example, a machine-readable medium may
30 include read-only memory (ROM), random-access memory (RAM), magnetic disk storage media, optical storage media, flash-memory devices, electrical, optical, acoustical or other form of propagated signals (e.g., carrier wave, infrared signals, digital signals, etc.), and others.

The Abstract is provided to comply with 37 C.F.R. Section 1.72(b) requiring an abstract that will allow the reader to ascertain the nature and gist of the technical disclosure. It is submitted with the understanding that it will not be used to limit or interpret the scope or meaning of the claims.

5 In the foregoing detailed description, various features are occasionally grouped together in a single embodiment for the purpose of streamlining the disclosure. This method of disclosure is not to be interpreted as reflecting an intention that the claimed embodiments of the subject matter require more features that are expressly recited in each claim. Rather, as the following claims
10 reflect, inventive subject matter lies in less than all features of a single disclosed embodiment. Thus the following claims are hereby incorporated into the detailed description, with each claim standing on its own as a separate preferred embodiment.